GaAs JFET Front-End MMICs for L-Band Personal Communications

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ABSTRACT

GaAs JFET low noise and low distortion amplifier and mixer MMICs for front-end use in L-band personal communications have been developed. These MMICs can be operated by a 3.0 V single biasing supply with a very low current dissipation of 4.0 mA. In order to achieve excellent low intermodulation distortion, a current mirror active biasing circuit using enhancement-mode JFETs, and a resistive mixing configuration were adopted.

INTRODUCTION

For GaAs MMICs used in a portable handset for personal communications, both low voltage biasing and low current dissipation are mandatory for battery operation. In addition, because the handset terminal is used in an environment where the intensity of the signal being received is constantly changing, a low intermodulation distortion is also required for the front-end MMICs. In this paper, the design and performance of low noise and low distortion amplifier and mixer MMICs for L-band front-end applications are described. These MMICs can be operated with a +3.0 V single biasing supply with a very low current dissipation of 4.0 mA. In order to achieve low intermodulation distortion, these MMICs were designed using enhancement-mode JFETs with an on-chip current mirror active biasing circuit, as well as an RC feedback for the second-stage of the low noise amplifier, and a resistive configuration for the mixer.

CIRCUIT DESIGN

The circuit configurations of the low noise amplifier and mixer MMICs are shown in Figure 1. The low noise amplifier is a two-stage type incorporating input, output, and interstage matching circuits. For the first-stage amplifier, a source inductor was used to achieve a simultaneous low noise figure and low input VSWR [1]. For the second-stage amplifier, RC feedback was used to suppress the gain, which lead to improved intermodulation distortion.

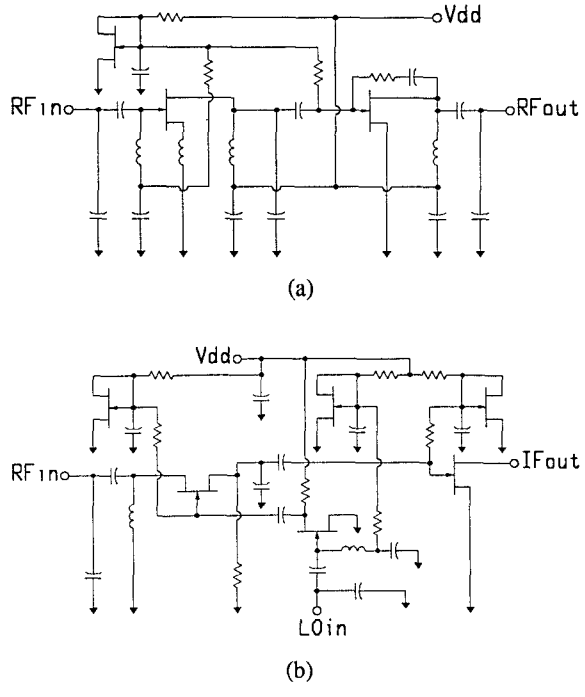

Figure 1. Circuit configurations of (a) low noise amplifier and (b) mixer.

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The problem of intermodulation distortion is more critical for a mixer IC than it is for the low noise amplifier because of the increased input signal level. In this case, a resistive mixing configuration was used to obtain low intermodulation distortion [2]. In order for the mixer IC to exhibit conversion gain at low LO power operation, LO and IF buffer amplifiers were incorporated. Matching circuits for the RF and LO inputs were also included within the chip.

LC π-type matching circuits were used for both MMICs to reduce the number of spiral inductors, which allowed a reduction in chip size.

For stabilizing the DC bias, a source resistance with a bypass capacitor for grounding is often used. However, through experimental investigation and simulation, it was discovered that this severely degraded the MMIC's intermodulation characteristics, if the capacitance was small. For example, the IM3 suppression ratio of the low noise amplifier was found to degrade by 14 dB when a 20 pF bypass capacitor and source resistance were used. To eliminate this, a much larger bypass capacitor on the order of 100 pF was required, but it was too large to be included monolithically on the chip. In order to overcome this problem, a current mirror active biasing circuit utilizing an enhancement-mode JFET similar to the one being used in the amplifer/mixer circuit, but with a smaller gate width of 15 μm, was used. The center of the threshold voltage was chosen to +0.3 V, where the drain current is most stable against fluctuations in the FET's threshold voltage. The low noise amplifier IC's total current dependence on threshold voltage are shown in Figure 2. The fluctuations of total current were less than ± 25 % for the range of threshold voltage 0.3 ± 0.2 V. Although an enhancement-mode JFET with a threshold voltage of 0.3 V shows a few tenths of a decibel higher noise figure compared with that of a depletion-mode JFET, this difference is not critical for this front-end application. As the junction FET has a high built-in gate voltage of 1.2 V, the MMICs can be operated without distortion even though FETs with a high threshold voltage of +0.3 V are used. This is one of the advantages of using JFETs.

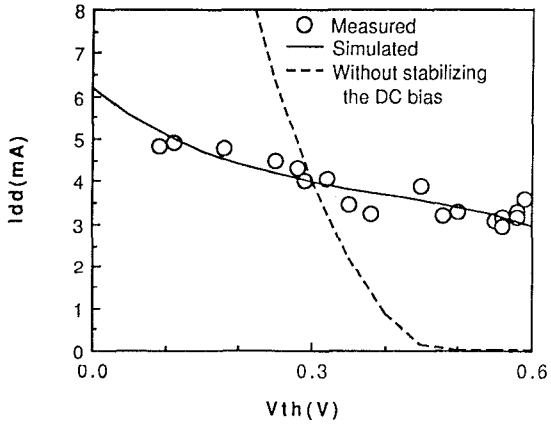
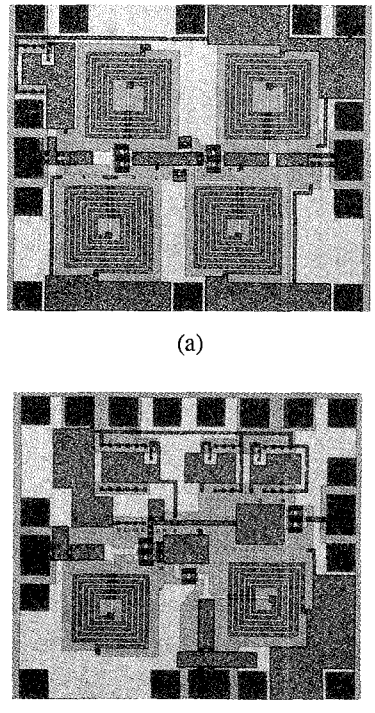


Figure 2. The low noise amplifier IC's total current dependence on threshold voltage.

FABRICATION

MMICs were fabricated on a 3-inch semi-insulating undoped LEC GaAs substrate. A p-layer was buried underneath the channel by Mg^+ implantation to suppress the short channel effects. Si implantation and capless annealing technique were used to form the n-channel and n^+ ohmic contact region. The p^+ gate region was formed by selective Zn diffusion using an open-tube reactor with DEZ(Diethyl-Zinc)[3]. The gate length was 0.5 μm by using optical



(a)

(b)

Figure 3. Microphotographs of (a) low noise amplifier and (b) mixer MMICs.

lithography and a sidewall assisted technique.

Resistor were also fabricated by Si implantation with the sheet resistance designed to be 300 Ω/□, and MIM capacitors were formed by sandwiching a 200 nm thick Si_3N_4 dielectric layer inside the two-level metal interconnection layer. Width/spacing and thickness of the spiral inductors were chosen to be 10 μm/10 μm, and 4 μm.

Microphotographs of the MMICs are shown in Figure 3. The gate width was chosen to be 200 μm for the low noise amplifier, mixer, and IF buffer amplifier FETs, and 100 μm for the LO buffer amplifier FET. As a result of the reduction of the number of inductors through the utilization of LC π-type matching circuits and the elimination of bypass capacitors for stabilizing the DC bias, chip sizes as small as 1.10 mm x 1.25 mm for the low noise amplifier and 1.10 mm x 1.20 mm for the mixer were achieved. When compared to results in recent publications, these chip sizes are very small for an L-band MMIC which includes matching circuits [4] [5].

PERFORMANCE

Typical frequency responses of the noise figure and gain of the low noise amplifier are shown in Figure 4. The noise figure was 2.8 dB with a gain of 18.1 dB at 1.9 GHz. The current dissipation was only 4.0 mA with a 3.0 V biasing supply. Figure 5 shows the intermodulation characteristics with 1.9/1.901 GHz two-tone input signals. The intercept point determined from the extrapolation of the plotted data at small input levels was 7 dBm. The deviation of the trace of third order intermodulation products from the theoretical line at

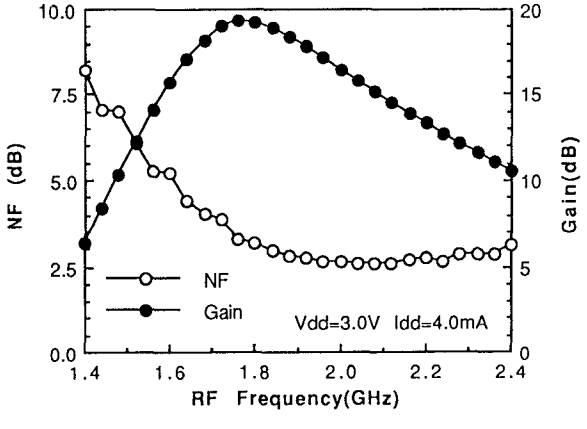


Figure 4. Frequency responses of noise figure and gain of low noise amplifier.

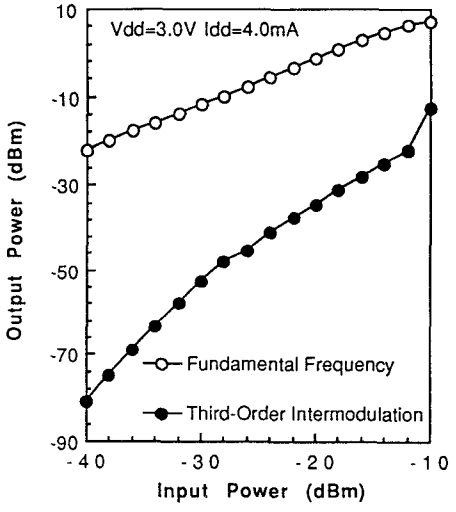


Figure 5. Intermodulation characteristics of low noise amplifier with 1.9/1.901 GHz two-tone input signals.

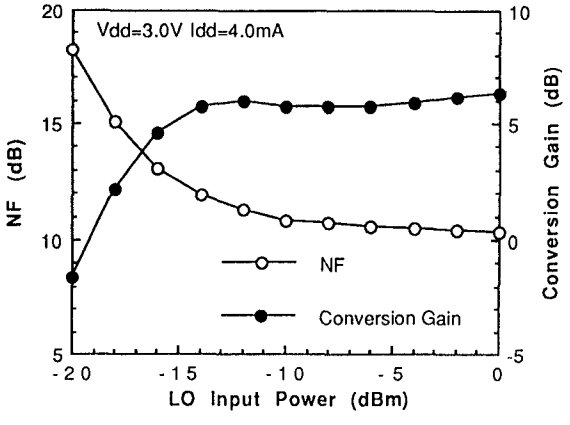


Figure 6. Dependence of mixer SSB noise figure and conversion gain on LO power.

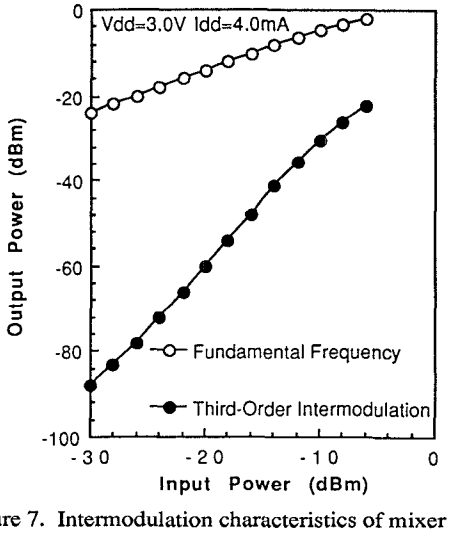


Figure 7. Intermodulation characteristics of mixer with 1.9/1.903 GHz two-tone input signals.

a high input level is due to the fact that the biasing point shifted to quasi class B operation.

Typical dependence of mixer SSB noise figure and conversion gain on LO power with external IF output matching circuits are shown in Figure 6. Here, the current dissipation was also 4.0 mA with a 3.0 V biasing supply, and the RF and LO frequencies were 1.9 and 1.66 GHz. The noise figure was 10.8 dB and the conversion gain was 5.7 dB with a low LO power of -10 dBm. Figure 7 shows the intermodulation characteristics with 1.9/1.903 GHz two-tone input signals. An intercept point of 8 dBm was achieved with a low current dissipation of 4.0 mA and a low LO power of -10 dBm.

CONCLUSION

The performances of the low noise amplifier and mixer MMICs are summarized in Table I. These MMICs not only satisfy the specifications for portable handsets for personal comunnications, but also have a wide variety of applications because of their excellent performance with very low power dissipation and small chip size.

Supply Voltage	3.0V
Current Dissipation	4.0mA
Frequency	1.9GHz
Noise Figure	2.8dB
Gain	18.1dB
IP3 (Output)	7dBm
Input VSWR	1.5
Output VSWR	3.1
Isolation	21dB

(a)

Supply Voltage	3.0V
Current dissipation	4.0mA
RF Frequency	1.9GHz
LO Frequency	1.66GHz
LO Input Power	-10dBm
SSB Noise Figure	10.8dB
Conversion Gain	5.7dB
IP3 (Output)	8dBm
RF VSWR	1.2
LO VSWR	1.2
LO-RF Isolation	13dB
LO-IF Isolation	5dB

(b)

Table I. Performance of (a) low noise amplifier and (b) mixer.

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